100307 Low Power Quint Exclusive OR/NOR Gate

General Description
The 100307 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs. All inputs have 50 k\(\Omega\) pull-down resistors.

Features
- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with 100107
- Voltage compensated operating range = \(-4.2\)V to \(-5.7\)V
- Available to industrial grade temperature range
- Available to Standard Microcircuit Drawing (SMD) 5962-9459001

Logic Symbol

Logic Equation
\[
F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})
\]

Pin Names
- \(D_{na} - D_{ne}\) Data Inputs
- \(F\) Function Output
- \(O_a - O_e\) Data Outputs
- \(\bar{O}_a - \bar{O}_e\) Complementary Data Outputs
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Above which the useful life may be impaired. (Note 1)
- Storage Temperature ($T_{STG}$) -65°C to +150°C
- Maximum Junction Temperature ($T_J$)
  - Ceramic +175°C
  - Plastic +150°C
- $V_{EE}$ Pin Potential to Ground Pin -7.0V to +0.5V
- Input Voltage (DC) $V_{EE}$ to +0.5V
- Output Current (DC Output HIGH) -50 mA

**ESD (Note 2)** ≥2000V

### Recommended Operating Conditions

- Case Temperature ($T_C$) Military -55°C to +125°C
- Supply Voltage ($V_{EE}$) -5.7V to -4.2V

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

### Military Version

### DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55°C$ to $+125°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>$T_C$ Conditions</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output HIGH Voltage</td>
<td>-1025</td>
<td>-870</td>
<td>mV</td>
<td>0°C to +125°C</td>
<td>Loading with 50Ω to −2.0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-1085</td>
<td>-870</td>
<td>mV</td>
<td>−55°C</td>
<td>$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output LOW Voltage</td>
<td>-1830</td>
<td>-1620</td>
<td>mV</td>
<td>0°C to +125°C</td>
<td>Loading with 50Ω to −2.0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-1830</td>
<td>-1555</td>
<td>mV</td>
<td>−55°C</td>
<td>$V_{IN} = V_{IL}$ (Max) or $V_{IH}$ (Min)</td>
</tr>
<tr>
<td>$V_{OHC}$</td>
<td>Output HIGH Voltage</td>
<td>-1035</td>
<td>mV</td>
<td>0°C to +125°C</td>
<td>Loading with 50Ω to −2.0V</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-1085</td>
<td>mV</td>
<td>−55°C</td>
<td>$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)</td>
<td></td>
</tr>
<tr>
<td>$V_{OLC}$</td>
<td>Output LOW Voltage</td>
<td>-1610</td>
<td>mV</td>
<td>0°C to +125°C</td>
<td>Loading with 50Ω to −2.0V</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-1555</td>
<td>mV</td>
<td>−55°C</td>
<td>$V_{IN} = V_{IL}$ (Max) or $V_{IH}$ (Min)</td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input HIGH Voltage</td>
<td>-1165</td>
<td>-870</td>
<td>mV</td>
<td>−55°C to +125°C</td>
<td>Guaranteed HIGH Signal for All Inputs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-1115</td>
<td>-870</td>
<td>mV</td>
<td>+125°C</td>
<td>Guaranteed LOW Signal for All Inputs</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input HIGH Current $D_{2a} - D_{2e}$</td>
<td>250</td>
<td>μA</td>
<td>−55°C to +125°C</td>
<td>$V_{EE} = -4.2V$</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>350</td>
<td>μA</td>
<td>+125°C</td>
<td>$V_{IN} = V_{IL}$ (Min)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$D_{1a} - D_{1e}$</td>
<td>350</td>
<td>μA</td>
<td>−55°C</td>
<td>$V_{EE} = -5.7V$</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500</td>
<td>μA</td>
<td>+125°C</td>
<td>$V_{IN} = V_{IL}$ (Max)</td>
<td></td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td>-75</td>
<td>mA</td>
<td>−55°C to +125°C</td>
<td>Inputs Open</td>
<td>1, 2, 3</td>
</tr>
</tbody>
</table>

**Note 3:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.

**Note 4:** Screen tested 100% on each device at −55°C, +25°C, and +125°C. Subgroups 1, 2, 3, 7, and 8.

**Note 5:** Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C. Subgroups A1, 2, 3, 7, and 8.

**Note 6:** Guaranteed by applying specified input condition and testing $V_{OH}$/$V_{OL}$.
### AC Electrical Characteristics

\( V_{EE} = -4.2\, \text{V to } -5.7\, \text{V}, \; V_{CC} = V_{CC1} = \text{GND} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>( T_C = -55, \text{˚C} )</th>
<th>( T_C = +25, \text{˚C} )</th>
<th>( T_C = +125, \text{˚C} )</th>
<th>Conditions</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay ( D_{2a} - D_{2e} ) to O, ( \overline{O} )</td>
<td>0.30</td>
<td>2.10</td>
<td>0.40</td>
<td>1.90</td>
<td>0.40</td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay ( D_{1a} - D_{1e} ) to O, ( \overline{O} )</td>
<td>0.80</td>
<td>2.90</td>
<td>0.90</td>
<td>2.80</td>
<td>0.90</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay Data to F</td>
<td>0.20</td>
<td>1.70</td>
<td>0.30</td>
<td>1.60</td>
<td>0.20</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Transition Time 20% to 80%, 80% to 20%</td>
<td>0.20</td>
<td>1.70</td>
<td>0.30</td>
<td>1.60</td>
<td>0.20</td>
</tr>
</tbody>
</table>

**Note 7:** P100K 200 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals \(-55\, \text{˚C}\)), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 8:** Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

**Note 9:** Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A8, and at +125°C and -55°C temperatures, Subgroups A10 and A11.

**Note 10:** Not tested at +25°C, +125°C, and -55°C temperature (design characterization data).

#### Test Circuitry

**FIGURE 1. AC Test Circuit**

Notes:
- \( V_{CC}, V_{CC1} = +2\, \text{V}, V_{EE} = -2.5\, \text{V} \)
- \( L_1 \) and \( L_2 \) = equal length 50Ω impedance lines
- \( R_T \) = 50Ω terminator internal to scope
- Decoupling 0.1 \( \mu \text{F} \) from GND to \( V_{CC} \) and \( V_{EE} \)
- All unused outputs are loaded with 50Ω to GND
- \( C_L \) = fixture and stray capacitance \( \leq 3 \, \text{pF} \)
Switching Waveforms

FIGURE 2. Propagation Delay and Transition Times
Physical Dimensions  inches (millimeters) unless otherwise noted

24-Pin Ceramic Dual-In-Line Package (D)
NS Package Number J24E

24-Pin Quad Cerpak (F)
NS Package Number W24B
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