100114
Line Receiver

Quint Differential Line Receiver
Product Specification

ECL Products

DESCRIPTION

The 100114 contains five gates with differential inputs and complementary outputs. An internal reference bias is available (V_{BB}), which enables, when connected to a gate input, the other to operate as a standard 100K ECL input. The direct output of a gate goes LOW, and the complementary one goes HIGH when both inputs are either open, or at V_{CC}, or have equal voltage applied.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT ($-I_{EE}$)
100114	1.40ns	73mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$ $T_A = 0°C$ to $+85°C$
Ceramic DIP	100114F
Ceramic Flat Pack	100114Y

PIN DESCRIPTION

PINS	DESCRIPTION
D_1, D_3, D_5, D_7, D_9	Data Inputs
$\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$, $\overline{D}_6$, $\overline{D}_8$	Inverting Data Inputs
$Q_0 - Q_4$, $\overline{Q}_0 - \overline{Q}_4$	Data Outputs

PIN CONFIGURATION

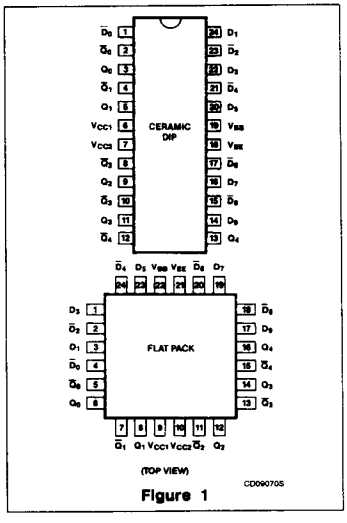

Figure 1

LOGIC SYMBOL

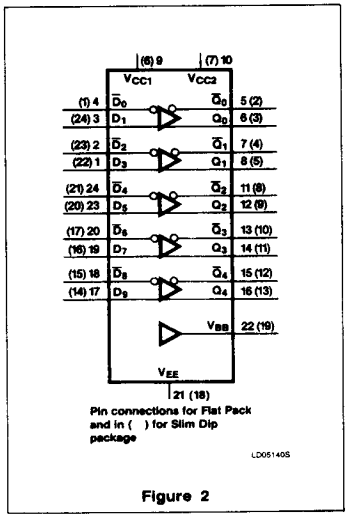

Figure 2

FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS	
$\overline{D}_0$	D_1	$\overline{Q}_0$	Q_1
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$V_{ID} \geq 0V$	$V_{ID} \geq 0V$	H	L
$V_{ID} \leq -0.150V$	$V_{ID} \leq -0.150V$	L	H
$-0.150V < V_{ID} < 0V$	$-0.150V < V_{ID} < 0V$	*	*
open	open	H	L
V_{CC}	V_{CC}	H	L

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
* = Indeterminate state
V_{BB} = Internal reference pin 22 (18)
V_{ID} = Complement to direct input voltage difference.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

	PARAMETER	100K ECL	UNIT
V_{EE}	Supply voltage ($V_{CC1} = V_{CC2} = GND$)	−7.0 to 0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current	−55	mA
T_S	Storage temperature	−65 to +150	°C
T_J	Maximum junction temperature	+150	°C

DC OPERATING CONDITIONS

PARAMETER				100K ECL Min	100K ECL Nom	100K ECL Max	UNIT
V_{CC1}, V_{CC2}	Circuit ground			0	0	0	V
V_{EE}	Supply voltage (negative)			−4.2	−4.5	−4.8	V
V_{EE}	Supply voltage (negative) when operating with 10K ECL family					−5.7	V
V_{IH}	HIGH level input voltage	$V_{CC1} = V_{CC2} = GND$, $T_A = 0°C$ to $+85°C$	$V_{EE} = -4.2V$	−1150		−880	mV
			$V_{EE} = -4.5V$	−1165			
			$V_{EE} = -4.8V$				
V_{IHT}	HIGH level input threshold voltage		$V_{EE} = -4.2V$	−1150			mV
			$V_{EE} = -4.5V$	−1165			mV
			$V_{EE} = -4.8V$				
V_{ILT}	LOW level input threshold voltage		$V_{EE} = -4.2V$			−1475	mV
			$V_{EE} = -4.5V$				
			$V_{EE} = -4.8V$			−1490	mV
V_{IL}	LOW level input voltage		$V_{EE} = -4.2V$				mV
			$V_{EE} = -4.5V$	−1810		−1475	
			$V_{EE} = -4.8V$			−1490	
V_{IHmax}	Minimum permissable HIGH level input voltage		$V_{EE} = -4.2V$				mV
			$V_{EE} = -4.5V$			−230	
			$V_{EE} = -4.8V$				
V_{REFmin}	Minimum permissable extended input reference voltage		$V_{EE} = -4.2V$				mV
			$V_{EE} = -4.5V$	−2300			
			$V_{EE} = -4.8V$				
V_{CM}	Common mode voltage	$V_{CC1} = V_{CC2} = GND$, $T_A = 0°C$ to $+85°C$, permissable $\pm V_{CM}$ with respect to V_{BB}	$V_{EE} = -4.2V$				V
			$V_{EE} = -4.5V$			1.0	
			$V_{EE} = -4.8V$				
V_{DIFF}	Differential input voltage	$V_{CC1} = V_{CC2} = GND$, $T_A = 0°C$ to $+85°C$, required for full swing output	$V_{EE} = -4.2V$				mV
			$V_{EE} = -4.5V$	150			
			$V_{EE} = -4.8V$				
T_A	Operating ambient temperature			0	+25	+85	°C

NOTE:
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

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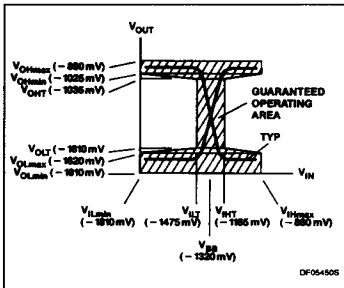
DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

PARAMETER			MIN	TYP	MAX	UNIT	TEST CONDITIONS[2]	
V_{OH}	HIGH level output voltage	$V_{EE} = -4.2V$	-1025		-870	mV	$V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$	Loading with 50Ω to -2.0V ±0.010V
		$V_{EE} = -4.5V$	-1025	-955	-880	mV		
		$V_{EE} = -4.8V$	-1035		-880	mV		
V_{OHT}	HIGH level output threshold voltage	$V_{EE} = -4.2V$	-1035			mV	$V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$	
		$V_{EE} = -4.5V$	-1035			mV		
		$V_{EE} = -4.8V$	-1045			mV		
V_{OLT}	LOW level output threshold voltage	$V_{EE} = -4.2V$			-1590	mV	$V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$	
		$V_{EE} = -4.5V$			-1610	mV		
		$V_{EE} = -4.8V$			-1610	mV		
V_{OL}	LOW level output voltage	$V_{EE} = -4.2V$	-1810		-1600	mV	$V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$	
		$V_{EE} = -4.5V$	-1810	-1705	-1620	mV		
		$V_{EE} = -4.8V$	-1830		-1620	mV		
V_{BB}	Output reference voltage	$V_{EE} = -4.5V$	-1380	-1320	-1260	mV	$I_{BB} = 0$ to 475µA	
		$V_{EE} = -4.2V$ to $-4.8V$	-1396	-1320	-1244	mV		
I_{IH}	HIGH level input current				65	µA	$V_{IN} = V_{IHmax}$, second input to V_{BB}	
I_{CBO}	Input leakage current		-10			µA	$V_{IN} = V_{EE}$, second input to V_{BB}	
$-I_{EE}$	V_{EE} supply current		51	73	106	mA	Inputs open	
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	HIGH level output voltage compensation	$V_{EE} = -4.2V$, $T_A = +25°C$			0.035	V/V		
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	LOW level output voltage compensation				0.07	V/V		

NOTES:

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.



NOTES:

V_{IHmax} – Maximum HIGH level input voltage (the most positive V_{IH}).
V_{IHT} – HIGH level input threshold voltage.
V_{ILT} – LOW level input threshold voltage.
V_{ILmin} – Minimum LOW level input voltage (the most negative V_{IL}).
V_{OHmax} – Maximum HIGH level output voltage (the most positive V_{OH}) under the specified input and loading condition.
V_{OHmin} – Minimum HIGH level output voltage (the most negative V_{OH}) under the specified input and loading condition.
V_{OHT} – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLT} – LOW level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLmax} – Maximum LOW level output voltage (the most positive V_{OL}) under the specified input and loading conditions.
V_{OLmin} – Minimum LOW level output voltage (the most negative V_{OL}) under the specified input and loading conditions.
V_{BB} – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 3. Transfer Characteristics

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	0.55	2.20	0.60	2.20	0.70	2.40	ns	Figs. 4, 5, 6
t_{PHL}	D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	0.55	2.20	0.60	2.20	0.70	2.40	ns	
t_{TLH}	Transition time	0.45	1.30	0.45	1.20	0.45	1.30	ns	
t_{THL}	20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	0.55	2.20	0.60	2.20	0.70	2.40	ns	Figs. 4, 5, 6
t_{PHL}	D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	0.55	2.20	0.60	2.20	0.70	2.40	ns	
t_{TLH}	Transition time	0.45	1.30	0.45	1.20	0.45	1.30	ns	
t_{THL}	20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	0.55	2.00	0.60	2.00	0.70	2.20	ns	Figs. 4, 5, 6
t_{PHL}	D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	0.55	2.00	0.60	2.00	0.70	2.20	ns	
t_{TLH}	Transition time	0.45	1.30	0.45	1.20	0.45	1.30	ns	
t_{THL}	20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	0.55	2.00	0.60	2.00	0.70	2.20	ns	Figs. 4, 5, 6
t_{PHL}	D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	0.55	2.00	0.60	2.00	0.70	2.20	ns	
t_{TLH}	Transition time	0.45	1.30	0.45	1.20	0.45	1.30	ns	
t_{THL}	20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

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AC WAVEFORMS

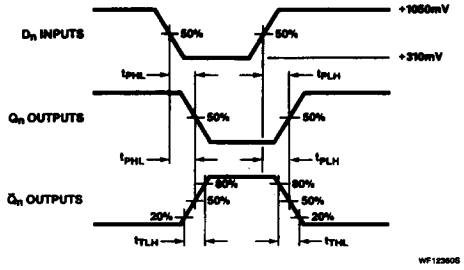
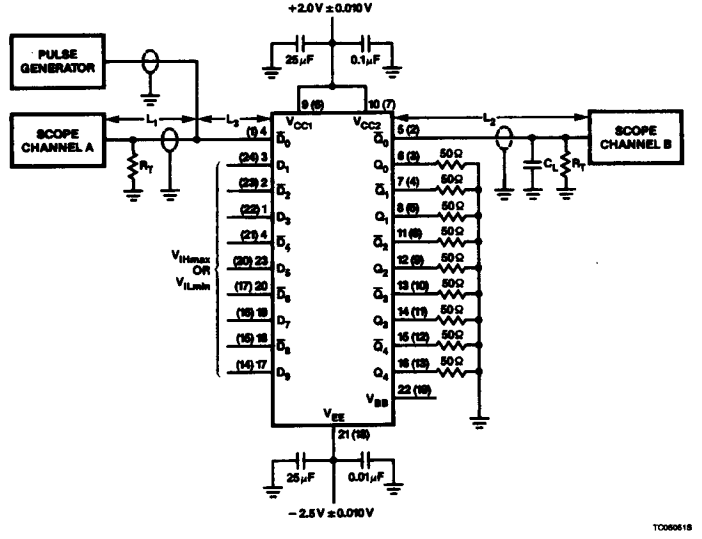


Figure 4. Propagation Delay and Transition Times

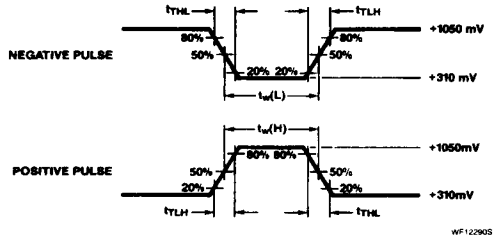
TEST CIRCUITS AND WAVEFORMS



NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_2, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω terminator internal to Scope
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance < 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 5. Test Circuit



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, V_T = GND (0V)					
Family	**Amplitude**	**Rep Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
100K ECL	740mVp-p	1MHz	500ns	0.7 ±0.1ns	0.7 ±0.1ns

Figure 6. Input Pulse Definition