Signetics

100141
Shift Register

8-Bit Shift Register
Product Specification

ECL Products

DESCRIPTION

100141 has eight D-type flip-flops, and two selection inputs, S_0, S_1, allowing a parallel loading or left shifting or right shifting, or hold operation mode.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT ($-I_{EE}$)
100141	1.7ns	175mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$ $T_A = 0°C$ to $+85°C$
Ceramic DIP	100141F
Ceramic Flat Pack	100141Y

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Serial Data Inputs
$P_0 - P_3$	Parallel Data Inputs
CP	Clock Input
S_0, S_1	Select Inputs
$Q_0 - Q_7$	Data Outputs

PIN CONFIGURATION

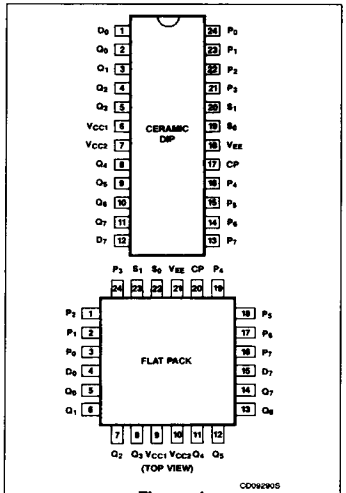

Figure 1

LOGIC SYMBOL

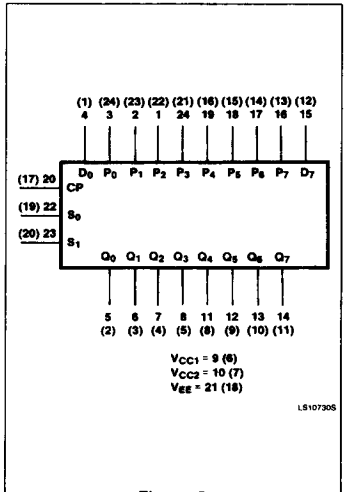

Figure 2

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LOGIC DIAGRAM

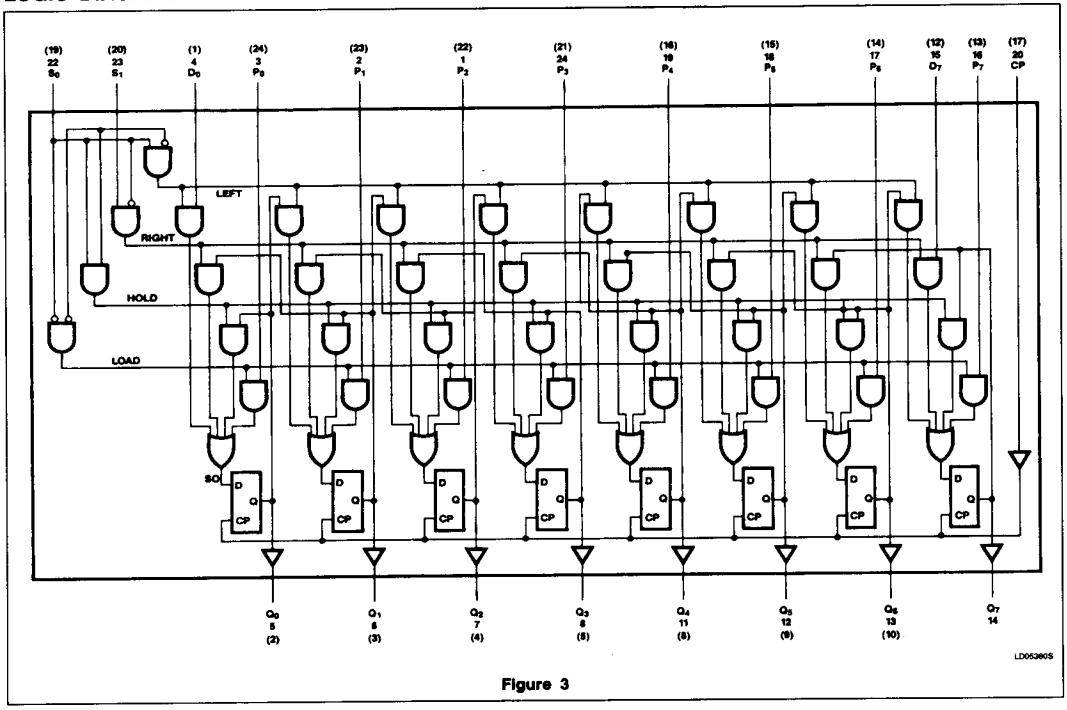

Figure 3

FUNCTION TABLE

MODE	INPUTS			OUTPUTS							
	S_0	S_1	CP	7 Q_{n+1}	6 Q_{n+1}	5 Q_{n+1}	4 Q_{n+1}	3 Q_{n+1}	2 Q_{n+1}	1 Q_{n+1}	0 Q_{n+1}
Register load	L	L	↑	7 P_n	6 P_n	5 P_n	4 P_n	3 P_n	2 P_n	1 P_n	0 P_n
Right shift	L	H	↑	7 D_n	7 Q_n	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n
Left shift	H	L	↑	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n	0 Q_n	0 D_n
Hold state	H	H	X	7 Q_n	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n	0 Q_n

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
↑ = LOW-to-HIGH transition
X = Don't Care
n = last state
n + 1 = next state after transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

PARAMETER		100K ECL	UNIT
V_{EE}	Supply voltage ($V_{CC1} = V_{CC2} = GND$)	−7.0 to 0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current	−55	mA
T_S	Storage temperature	−65 to +150	°C
T_J	Maximum junction temperature	+150	°C

DC OPERATING CONDITIONS

PARAMETER				100K ECL			UNIT
				Min	Nom	Max	
V_{CC1}, V_{CC2}	Circuit ground			0	0	0	V
V_{EE}	Supply voltage (negative)			−4.2	−4.5	−4.8	V
V_{EE}	Supply voltage (negative) when operating with 10K ECL family					−5.7	V
V_{IH}	HIGH level input voltage	$V_{CC1} = V_{CC2} = GND$	$V_{EE} = -4.2V$	−1150		−880	mV
			$V_{EE} = -4.5V$	−1165			
			$V_{EE} = -4.8V$				
V_{IHT}	HIGH level input threshold voltage		$V_{EE} = -4.2V$	−1150			mV
			$V_{EE} = -4.5V$	−1165			mV
			$V_{EE} = -4.8V$				
V_{ILT}	LOW level input threshold voltage	$T_A = 0°C$ to +85°C	$V_{EE} = -4.2V$			−1475	mV
			$V_{EE} = -4.5V$				
			$V_{EE} = -4.8V$			−1490	mV
V_{IL}	LOW level input voltage		$V_{EE} = -4.2V$	−1810		−1475	mV
			$V_{EE} = -4.5V$				
			$V_{EE} = -4.8V$			−1490	
T_A	Operating ambient temperature			0	+25	+85	°C

NOTE:
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

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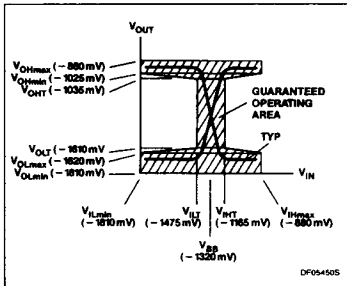
DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

PARAMETER			MIN	TYP	MAX	UNIT	TEST CONDITIONS[2]	
V_{OH}	HIGH level output voltage	$V_{EE} = -4.2V$	-1025		-870	mV	$V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$	Loading with 50Ω to $-2.0V \pm 0.010V$
		$V_{EE} = -4.5V$	-1025	-955	-880	mV		
		$V_{EE} = -4.8V$	-1035		-880	mV		
V_{OHT}	HIGH level output threshold voltage	$V_{EE} = -4.2V$	-1035			mV	$V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$	
		$V_{EE} = -4.5V$	-1035			mV		
		$V_{EE} = -4.8V$	-1045			mV		
V_{OLT}	LOW level output threshold voltage	$V_{EE} = -4.2V$			-1590	mV	$V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$	
		$V_{EE} = -4.5V$			-1610	mV		
		$V_{EE} = -4.8V$			-1610	mV		
V_{OL}	LOW level output voltage	$V_{EE} = -4.2V$	-1810		-1600	mV	$V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$	
		$V_{EE} = -4.5V$	-1810	-1705	-1620	mV		
		$V_{EE} = -4.8V$	-1830		-1620	mV		
I_{IH}	HIGH level input current	CP			640	μA	$V_{IN} = V_{IHmax}$	
		D_n, P_n, S_n			220	μA		
I_{IL}	LOW level input current		0.5			μA	$V_{IN} = V_{ILmin}$	
$-I_{EE}$	V_{EE} supply current		120	175	238	mA	Inputs open	
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	HIGH level output voltage compensation	$V_{EE} = -4.2V$, $T_A = +25°C$			0.025	V/V		
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	LOW level output voltage compensation				0.050	V/V		

NOTES:

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



NOTES:

V_{IHmax} – Maximum HIGH level input voltage (the most positive V_{IH}).
V_{IHT} – HIGH level input threshold voltage.
V_{ILT} – LOW level input threshold voltage.
V_{ILmin} – Minimum LOW level input voltage (the most negative V_{IL}).
V_{OHmax} – Maximum HIGH level output voltage (the most positive V_{OH}) under the specified input and loading condition.
V_{OHmin} – Minimum HIGH level output voltage (the most negative V_{OH}) under the specified input and loading condition.
V_{OHT} – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLT} – LOW level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLmax} – Maximum LOW level output voltage (the most positive V_{OL}) under the specified input and loading conditions.
V_{OLmin} – Minimum LOW level output voltage (the most negative V_{OL}) under the specified input and loading conditions.
V_{BB} – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum shift frequency	275		275		275		MHz	Figs. 5, 8, 9
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	0.90 0.90	2.40 2.40	1.10 1.10	2.40 2.40	1.10 1.10	2.55 2.55	ns ns	Figs. 5, 7, 9
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns	
t_s	Setup time D_n, P_n to CP	1.40		1.40		1.70		ns	Figs. 6, 9
t_h	Hold time D_n, P_n to CP	0.60		0.60		0.60		ns	
t_s	Setup time S_n to CP	3.80		3.80		3.40		ns	Figs. 6, 9
t_h	Hold time S_n to CP	0.10		0.10		0.10		ns	
$t_w(H)$	Pulse width HIGH CP	2.50		2.50		2.50		ns	Figs. 5, 9

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AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum shift frequency	275		275		275		MHz	Figs. 5, 8, 9
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	0.90 0.90	2.40 2.40	1.10 1.10	2.40 2.40	1.10 1.10	2.55 2.55	ns ns	Figs. 5, 7, 9
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns	
t_s	Setup time D_n, P_n to CP	1.40		1.40		1.70		ns	Figs. 6, 9
t_h	Hold time D_n, P_n to CP	0.60		0.60		0.60		ns	
t_s	Setup time S_n to CP	3.80		3.80		3.40		ns	Figs. 6, 9
t_h	Hold time S_n to CP	0.10		0.10		0.10		ns	
$t_w(H)$	Pulse width HIGH CP	2.50		2.50		2.50		ns	Figs. 5, 9

Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum shift frequency	300		300		300		MHz	Figs. 5, 8, 9
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	0.90 0.90	2.20 2.20	1.10 1.10	2.20 2.20	1.10 1.10	2.35 2.35	ns ns	Figs. 5, 7, 9
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns	
t_s	Setup time D_n, P_n to CP	1.20		1.20		1.50		ns	Figs. 6, 9
t_h	Hold time D_n, P_n to CP	0.50		0.50		0.50		ns	
t_s	Setup time S_n to CP	2.80		2.80		3.20		ns	Figs. 6, 9
t_h	Hold time S_n to CP	0.00		0.00		0.00		ns	
$t_w(H)$	Pulse width HIGH CP	2.50		2.50		2.50		ns	Figs. 5, 9

AC ELECTRICAL CHARACTERISTICS

Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

PARAMETER		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum shift frequency	300		300		300		MHz	Figs. 5, 8, 9
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	0.90 0.90	2.20 2.20	1.10 1.10	2.20 2.20	1.10 1.10	2.35 2.35	ns ns	Figs. 5, 7, 9
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns	
t_s	Setup time D_n, P_n to CP	1.20		1.20		1.50		ns	Figs. 6, 9
t_h	Hold time D_n, P_n to CP	0.50		0.50		0.50		ns	
t_s	Setup time S_n to CP	2.80		2.80		3.20		ns	Figs. 6, 9
t_h	Hold time S_n to CP	0.00		0.00		0.00		ns	
$t_w(H)$	Pulse width HIGH CP	2.50		2.50		2.50		ns	Figs. 5, 9

AC WAVEFORMS

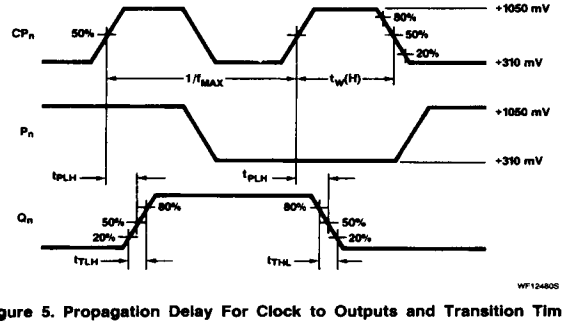


Figure 5. Propagation Delay For Clock to Outputs and Transition Times

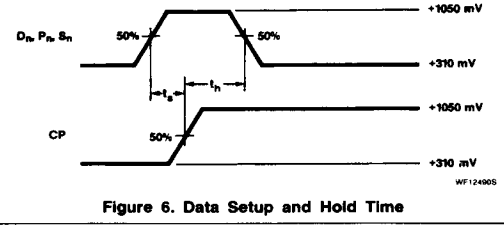
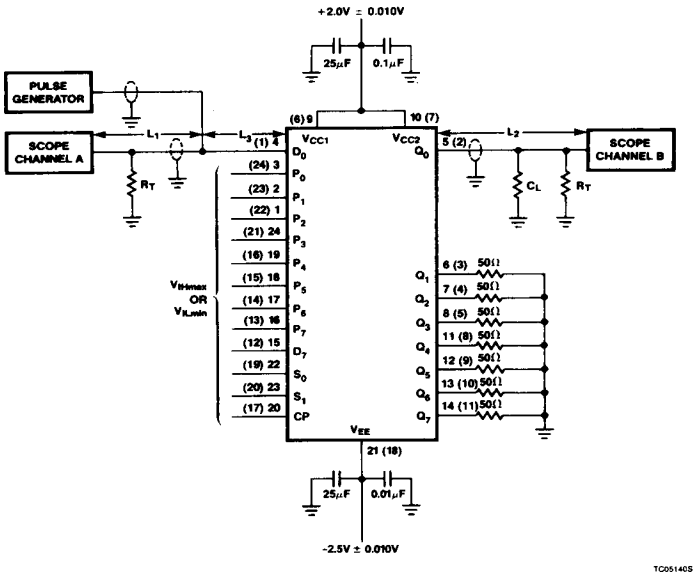


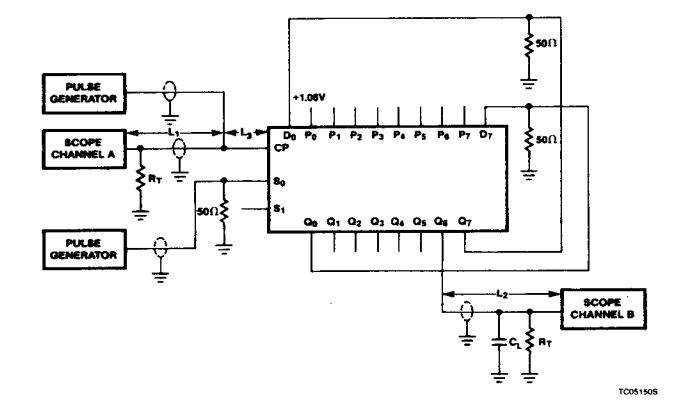
Figure 6. Data Setup and Hold Time

TEST CIRCUITS AND WAVEFORMS



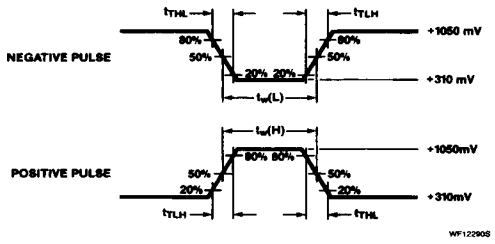
NOTES:
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pins connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 7. Test Circuit



NOTES:
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pins connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 8. Shift Frequency Test Circuit (Shift Left)



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, V_T = GND (0V)					
Family	**Amplitude**	**Rep Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
100K ECL	740mVp-p	1MHz	500ns	0.7 ±0.1ns	0.7 ±0.1ns

Figure 9. Input Pulse Definition

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